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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/483,101
Filing Date: January 14, 2000
Appellant(s): MCGRATH ET AL.

Lawrence J. Merkel
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02 September 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Examiner acknowledges that Applicant has grouped claim 1 separately from claim 17, whereby claim 1 rises and falls alone and claim 17 rises and falls alone. However, the Board is advised that the Applicant has failed to include reasons to support the grouping. Applicant has not explained how the two groups of claims differ in scope and are patentably distinct from each other. See 37 CFR 1.192(c)(7). Examiner notes that claim 1 is a device claim and claim 17 is a

related method claim. Examiner also notes that in the arguments section of the Appeal Brief, Applicant refers to the arguments and teachings of claim 1 when arguing claim 17.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Turley, James L. Advanced 80386 Programming Techniques. Berkeley, California: McGraw-Hill Inc., ©1988. Chapters 1, 2, 4, and 5.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 and 17 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

Referring to claim 1, Turley has taught a processor comprising:

A segment register configured to store a segment selector (Turley Page 47, Paragraph 3 and Page 63, Paragraph 4) identifying a segment descriptor (Turley Page 48, Paragraph 1 and Page 63, Paragraph 4) including a first operating mode indication (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57), a second operating mode indication (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57), and one or more bits identifying a segment described by said segment descriptor as a code segment (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57);

A control register configured to store an enable indication (Turley Page 26, Control Register 0, element PE), wherein said processor is configured to establish a

default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3).

Referring to claim 17, Turley has taught a method comprising:

Establishing a default address size in a processor (Turley Page 48, Paragraph 3 and Page 178, Paragraphs 2-3) in response an enable indication in a control register within said processor (Turley Page 26, Control Register 0, element PE; Page 176, Paragraph 1; and Page 178, Paragraph 2-3), a first operating mode indication in a segment descriptor (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57), a second operating mode indication in said segment descriptor (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57), said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment (Turley Page 49, Table A segment descriptor; Page 50-54; and Page 57); and

Generating addresses of said default address size (Turley Page 52, Paragraph 2).

The claims describe elements within the segment descriptor and control register needed to determine a default address size, and that two operating mode indications and an enable are used to produce a default address size. However, there is no description about how the operating mode indications and enable indication interact, just a statement that interaction occurs. The details of the interaction, i.e. how the indications are explicitly used to define a default address size, are provided in the dependent claims, which have been objected to as being dependent on a rejected claim but containing allowable subject matter. Also, the claim language does not

specify exactly what "address size" refers to, because "address size" could refer to the size of the address space or the number of bits needed to represent a valid address.

In order to clarify how Applicant's claims correspond to Turley, the examiner has mapped limitations of claim 1 to the device described in Turley with further explanation of the cited art.

Limitation in Question from Claim 1	***Corresponding Limitation in the Turley Reference for the Rejection of the Limitation***
A segment register configured to store a segment selector	Turley states on page 63, paragraph 4, "An 16-bit value that you write into a segment register is called a *selector*". This indicates that a value stored in a segment register is a segment selector.
Identifying a segment descriptor including	Turley states on page 63, paragraph 4, "...because it [the segment selector] selects a segment descriptor". This indicates that the segment selector identifies a segment descriptor.
A first operating mode indication	Turley shows in the table "A segment descriptor" on page 49 that there are various parts to a segment descriptor, including the segment's privilege level, which the examiner considers to be the first operating mode indication. On pages 10, 46-47, and 51, Turley states that the descriptor privilege level (DPL) indicates whether the application can access certain parts of memory, including whether the segment of memory is accessible.

A second operating mode indication, and	Turley shows in Figure 2-2 on page 50 that there is a G bit in the segment descriptor and describes its function further on page 47, paragraph 3; page 52, G; and page 54, paragraphs 2-3. To summarize, the granularity (G) bit is used as the default for determining the address size represented by the limit field. The limit field indicates the maximum number of addressable values in the address space, and the G bit indicates whether the limit field is a factor of 1 byte or 4096 bytes. Further explanation is provided below in response to Applicant's arguments.
One or more bits identifying a segment described by said segment descriptor as a code segment;	Turley shows in Figure 2-2 on page 50 that there is a Type field in the segment descriptor and describes its function further on page 51, Type and pages 55-57. As clearly stated on page 51 in **Type**, the Type field indicates which type of segment is defined, one type of which is the code segment (Turley Page 52, Type).
A control register configured to store an enable indication,	Turley shows on page 26, Control Register 0, PE that indicates whether Real mode is enabled or Protected mode is enabled, which is needed to implement segmentation in the manner described, as stated in Turley on page 45 in paragraph 2 "Second there is the method of segmentation used in protected mode" and page 47 in paragraph 2 "...concept of a segment is very different on an 80386 system running in Protected mode".

Wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.	Applicant does not provide details in this claim on how the enable indication, first operating mode indication, and second operating mode indication interact to establish a default address size. Applicant has only claimed that these three indications are used in some undefined way to establish the default address size. The signals indicated above interact in the following manner to establish a default address size. First, the PE bit in Control Register 0 must be set to enable protected mode (Turley page 26, Control Register 0, PE) in order for segmentation to even be possible (Turley page 45, paragraph 2 "...the method of segmentation used in Protected mode" and page 47, paragraph 2 "...concept of a segment...running in Protected mode"). In essence, when the PE bit is not set, the segmentation described is disabled and, when the PE bit is set, the segmentation is enabled. Second, the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size. Finally, the G bit establishes the address size, since it is used as the default for determining the address size represented by the Limit field. The G bit indicates whether the address space size spans one megabyte (1MB) of space or up to four gigabytes (4GB) of space. Therefore, in order to establish a default address size, Protected mode must be enabled by the PE bit, the DPL bit must indicate that segment memory is accessible, and the G bit is accessed to establish the address size.

The following shows what the examiner considers equivalent limitations found in claim 1, which is the device claim of the apparatus, and in claim 17, which is the method claim of the same apparatus. The rejection used for the limitation in claim 1 explained in detail in the above table and in the response to arguments below applies to the equivalent limitation in claim 17.

Limitation in Claim 1 (The device claim)	***Equivalent Limitation in Claim 17 (The method claim)***
A segment register configured to store a segment selector	
Identifying a segment descriptor including	A segment descriptor
A first operating mode indication	A first operating mode indication in a segment descriptor, and
A second operating mode indication, and	A second operating mode indication in said segment descriptor,
One or more bits identifying a segment described by said segment descriptor as a code segment;	Said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment;
A control register configured to store an enable indication,	An enable indication in a control register within said processor,

Wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.	Establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor... and Generating addresses of said default address size.

(11) Response to Argument

Examiner notes that Appellant only submitted one copy of the Appeal Brief. Examiner has made two extra copies of the Appeal Brief in order to prevent delay in the prosecution of the case. For future reference, Appellant is required to provide copies of the Appeal Brief in triplicate as stated in 37 CFR 1.192(a).

On pages 4-5 of the Appeal Brief, Applicant argues in essence:

> *"...Thus, the granularity bit, in conjunction with the limit field, defines the size of a segment. This does not teach or suggest a second operation mode indication 'wherein said processor is configured to* establish a default address size *responsive to said enable indication, said first operating mode indication, and* said second operating mode indication*'.*
>
> *...The G bit determines how to interpret the limit field, and defines the size of the segment. Addresses of the default address size (which is NOT determined by the*

G bit) would be used to address the segment, independent of the value of the G bit."

Figure 1 below has been provided to assist in the explanation of how the granularity (G) bit affects the default size of the address space and the default size of the effective address. The operation of the G bit is easier to explain and understand through an example scenario. The address space size set by the G bit determines how the limit address field is read by determining whether the limit is read in 1 byte or 4096 bytes (4KB) (Turley page 50 and page 54). The default address space size affected by the G bit is the number of values in the addressable region, i.e. how large the address space is (Turley page 50 and page 54). As seen in Figure 1 below, the G bit is used as the default for determining the address space size represented by the Limit field. Figure 1 illustrates what happens when the G bit is set to zero, labeled with "When G = 0 " and when it is set to one, labeled with "When G = 1". For the purposes of this explanation, the Base has been arbitrarily set to equal zero, which means that the first address referenced in the address space is at location zero, and the Limit has been arbitrarily set to equal one hundred. It is also useful to know that, in general, the following equations are used to find what the actual Limit, also known as the maximum address location, is and the address space size (Turley page 50 and page 54).

Actual Limit = Limit Field * G bit measurement

Address Space Size = Actual Limit - Base

Referring to "When G = 0", the Limit field is measured in 1 byte. The Limit field now denotes that the maximum address that can be accessed is address 100. The address space size is equal to 100 bytes, because addresses 0 to 100 are the only locations accessible. Referring to

"When G = 1", the Limit field is measured in 4096 bytes. The Limit field now denotes that the maximum address that can be accessed is address 409,600. The address space size is equal to 409,600 bytes, because addresses 0 to 409,600 are the only locations accessible. As shown in the example above and in Figure 1, the address space size has increased by 409,500 bytes when the G bit sets the default address space size to be determined in 4096 bytes instead of 1 byte.

Figure 2 shows the 20-bit representation of the maximum addresses shown in Figure 1. When G = 0, the maximum address is 100, and the binary representation of this decimal number only requires 7 bits for an effective address size, as can be seen under "When G = 0, Limit = 100". When G = 1, the maximum address is 409,600, and the binary representation of this decimal number requires 19 bits for an effective address size, as can be seen under "When G = 1, Limit = 409,600". The "X" bits following bit positions 6 and 19 represents bits that, when set to anything other than zero, produce illegal effective addresses (Turley page 50 and 54), because the effective address produced when any of these bits are set will always be outside the address space size defined by the G bit and Limit field (Turley page 50 and page 54). Therefore, the effective address size, when G = 0 and Limit = 100, is seven bits, because any more bits than that would create an address location too large for the address space defined, and, the effective address size, when G = 1 and Limit = 100, is nineteen bits, because any more bits than that would create an address location too large for the address space defined.

Figure 1

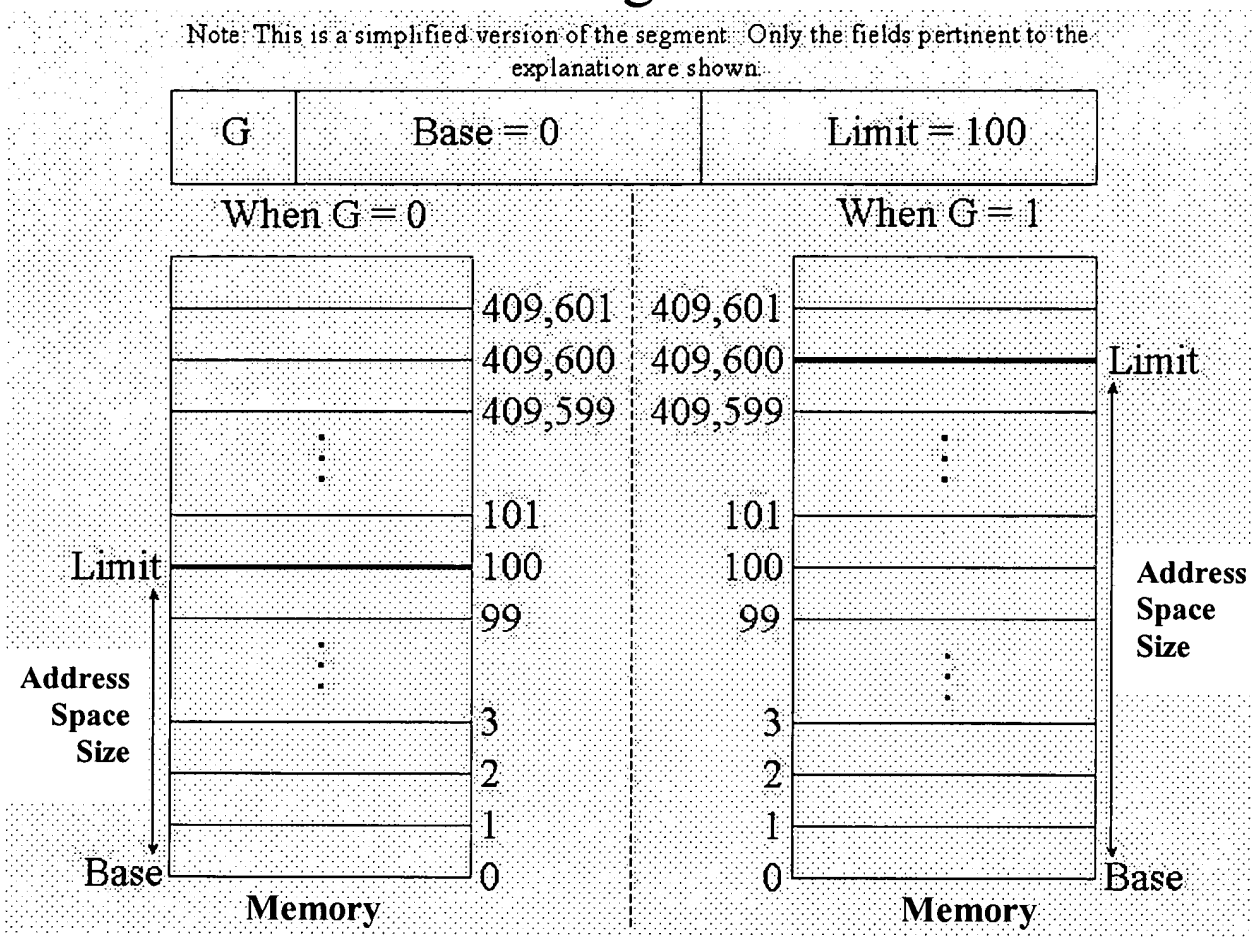
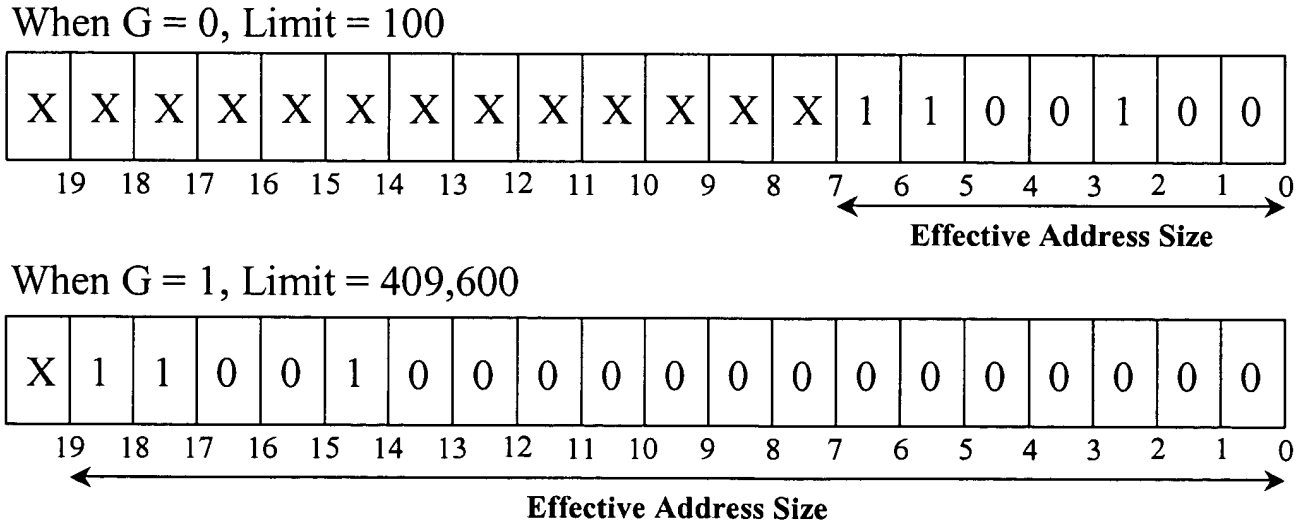


Figure 2



On page 4 of the Appeal Brief, Applicant argues in essence:

> *"With regard to the privilege level (DPL), Appellants respectfully submit that Turley has no teaching or suggestion that the DPL is in any way related to default address size. ... Thus, the privilege level may be used in determining if a memory access is granted or denied. Applicants respectfully submit that there is no teaching or suggestion in Turley that the privilege level is a first operating mode indication 'wherein said processor is configured to* establish a default address size *responsive to said enable indication,* said first operating mode indication, *and said second operating mode indication."*

Applicant's claim does NOT explicitly indicate the inter-relationships between the operating mode indications and enable indication, so it does not explicitly state that an operating mode indication has to have any direct effect on the address size. Whether memory access is granted or denied affects the default address size, because if the DPL indicates that the segment of memory cannot be accessed, then the default address size cannot be set (Turley page 46, paragraph 4 to page 47, paragraph 1 and page 51, DPL). When the DPL does not allow access to the memory segment, a new default address size cannot be set, since information from the segment, specifically the G bit, is required. Also, if the DPL indicates that certain areas of the memory space defined by the G bit are not accessible (Turley page 46, paragraph 4 to page 47, paragraph 1 and page 51, DPL), the address space size is decreased since those locations are no longer usable by an application. Therefore, the DPL is a first mode indication bit. The DPL indicates which memory access mode the system is in, thereby determining if it is even possible

to set a new default address size and whether the space defined is accessible (Turley page 46, paragraph 4 to page 47, paragraph 1 and page 51, DPL).

On page 5 of the Appeal Brief, Applicant argues in essence:

> *"The last sentence of item 9 in the Final Office Action states that 'Applicants admit in their argument that there is an enable indication for the default address size'. The Advisory Action states that 'Applicants have admitted that the D bit, or enable indication, deals with the default address size' (See Advisory Action, continuation sheet, last paragraph). Applicants respectfully disagree with the alleged admission. Nothing in Applicants' remarks is an admission as alleged in the Final Office Action and the Advisory Action. The mere statement that the D bit may have be [sic] related to address size is NOT an admission that the D bit is the claimed enable indication: 'a control register configured to store an enable indication'."*

The examiner did not intend to state or insinuate that Applicant has admitted that the D bit is the claimed enable indication. The examiner meant that Applicant has admitted that the D bit is related to the default address size, and, accordingly, the D bit could possibly be inferred as *an* enable indication. This does not indicate that the examiner believes that Applicant has admitted that the D bit is the *claimed* enable indication. The examiner has actually referred to the PE element of Control Register 0 as the claimed enable indication, as shown in the rejection above. Also, the examiner has attached a copy of Intel, page 11-13, paragraph 3, as cited by Applicant in paper number 13, Amendment B, page 5, paragraph 3 to page 6, paragraph 1 for extrinsic evidence showing that the D bit is related to the default address to support that the D

bit could possibly be inferred as an enable indication, because Turley does not explicitly say that the D bit is related to the default address. The copy of Intel has been provided to show that the D bit does affect address size.

On page 6 of the Appeal Brief, Applicant states in essence:

> *"The Final Office Action also refers to page 178, paragraphs 2 and 3 of Turley. This section of Turley describes the use of task state segments (TSS), and appears to have nothing to do with the above highlighted features..."*

The examiner wishes to point out that these pages cited were given to Applicant as additional information about the cited art.

On page 6 of the Appeal Brief, Applicant argues in essence:

> *"The Final Office Action relies on the same teachings from Turley to allegedly teach the first and second operating modes in claim 17 as were relied on for claim 1 (namely, the DPL, the G bit, page 49, table: A segment descriptor; pages 50-54; and page 57). These teachings, highlighted above in regard to claim 1, also do not teach or suggest the first operating mode indication and the second operating mode indication recited in claim 17."*

Please refer to the above in regard to the responses to the arguments presented in claim 1.

On pages 6-7 of the Appeal Brief, Applicant argues in essence:

> *"Additionally, the Final Office Action cites Turley's page 176, paragraph 1 and page 178, paragraphs 2-3 with regard to 'in response to an enable indication in a control register within said processor' as recited in claim 17. However, pages 176, paragraph 1 and page 178, paragraphs 2-3 describe the task state segment*

(TSS) and how it can be used for task switching. This has nothing to do with the above highlighted features, nor 'establishing a default address size in a processor in response to an enable indication in a control register within said processor...' as recited in claim 17."

Turley's page 176, paragraph 1 and page 178, paragraphs 2-3 were cited for further explanation of the art. This was supplied in order to provide Applicant with more detailed information regarding certain aspects of the art cited.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Aimee J. Li

October 20, 2003

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